

GA-MA790GP-DS4H *Revision : 1.0*

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRII CHANNEL A
09	DDRII CHANNEL B
10	DDRII TERMINATOR
11	RS780 HT-LINK I/F
12	RS780 PCIE I/F ,SWITCH
13	RS780 SYSTEM I/F
14	RS780 STRAPS ,SPMEM
15	RS780 POWER & GND
16	ICS9LPRS477
17	ATI SB750 PCIE/PCI/CPU/LPC
18	ATI SB750 ACPI/USB/GPIO/AUDIO
19	ATI SB750 SATA/SPI/IDE/HWM
20	ATI SB750 POWER & GND
21	PCI EXPRESS x16 ,x1
22	PCI SLOT 1, 2
23	RGB CONNECTOR
24	IDE ,FDD ,HDMI ,DVI Connector
25	COM/LPT/F_USB

[illegible]

Model Name:GA-MA790GP-DS4H

Component value change history


Version: 1.0

P-Code: U97027-0

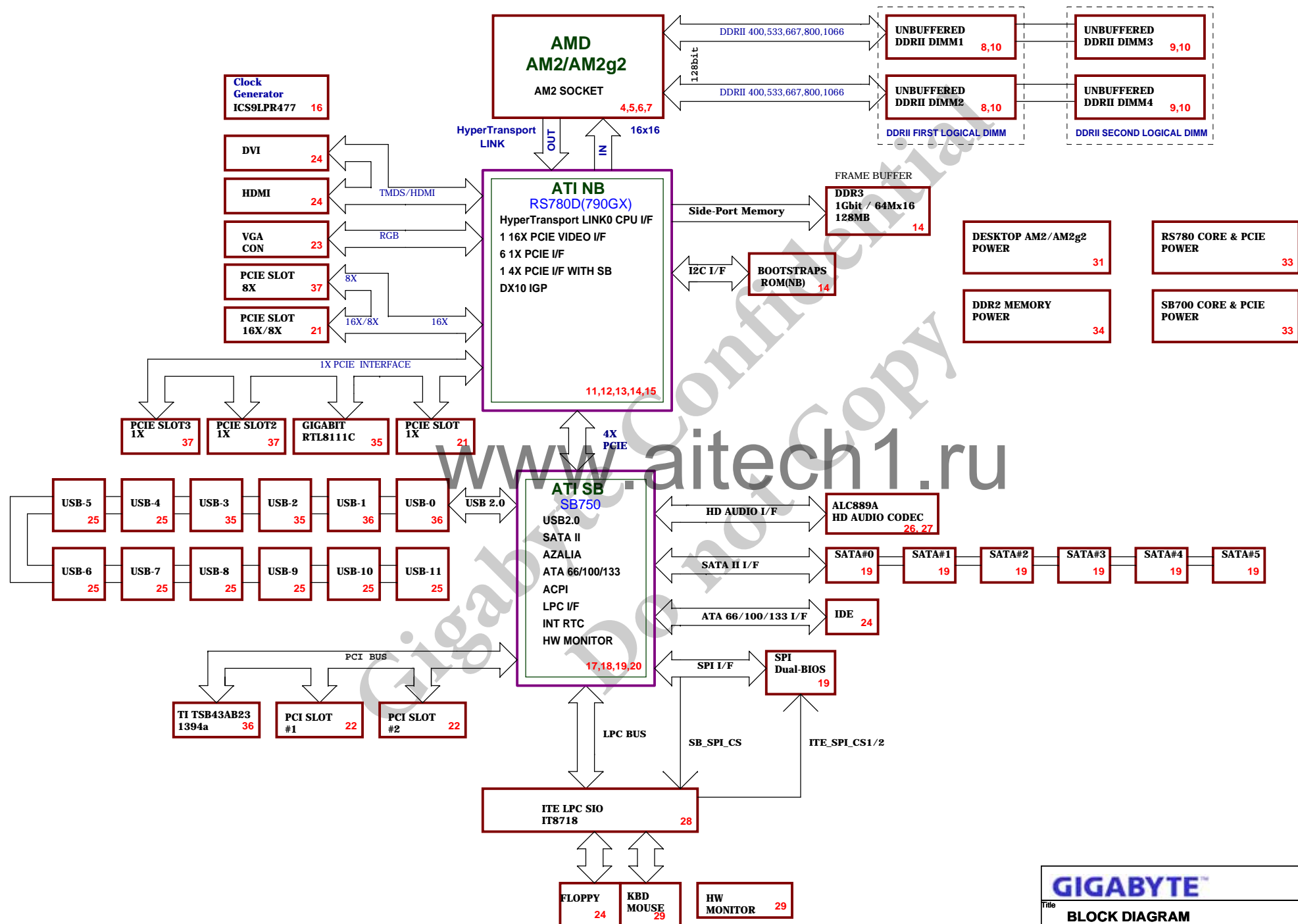
[illegible]

Circuit or PCB layout change for next version

[illegible]

				
Title				
BOM & PCB HISTORY				
Size	Document Number			Rev
Custom	GA-MA790GP-DS4H			1.0
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RS780 CUSTOMER DESKTOP REFERENCE DESIGN



L0_CADIN_L[0..15] L0_CADIN_L[0..15] 11
L0_CADIN_H[0..15] L0_CADIN_H[0..15] 11

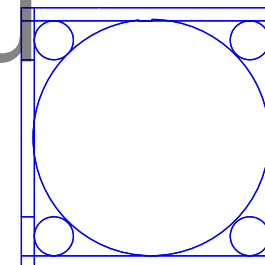
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 11
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 11

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B



SOCKET_M2
AM2RM/PP/OR/PB/[12KRC-04K807-03R]



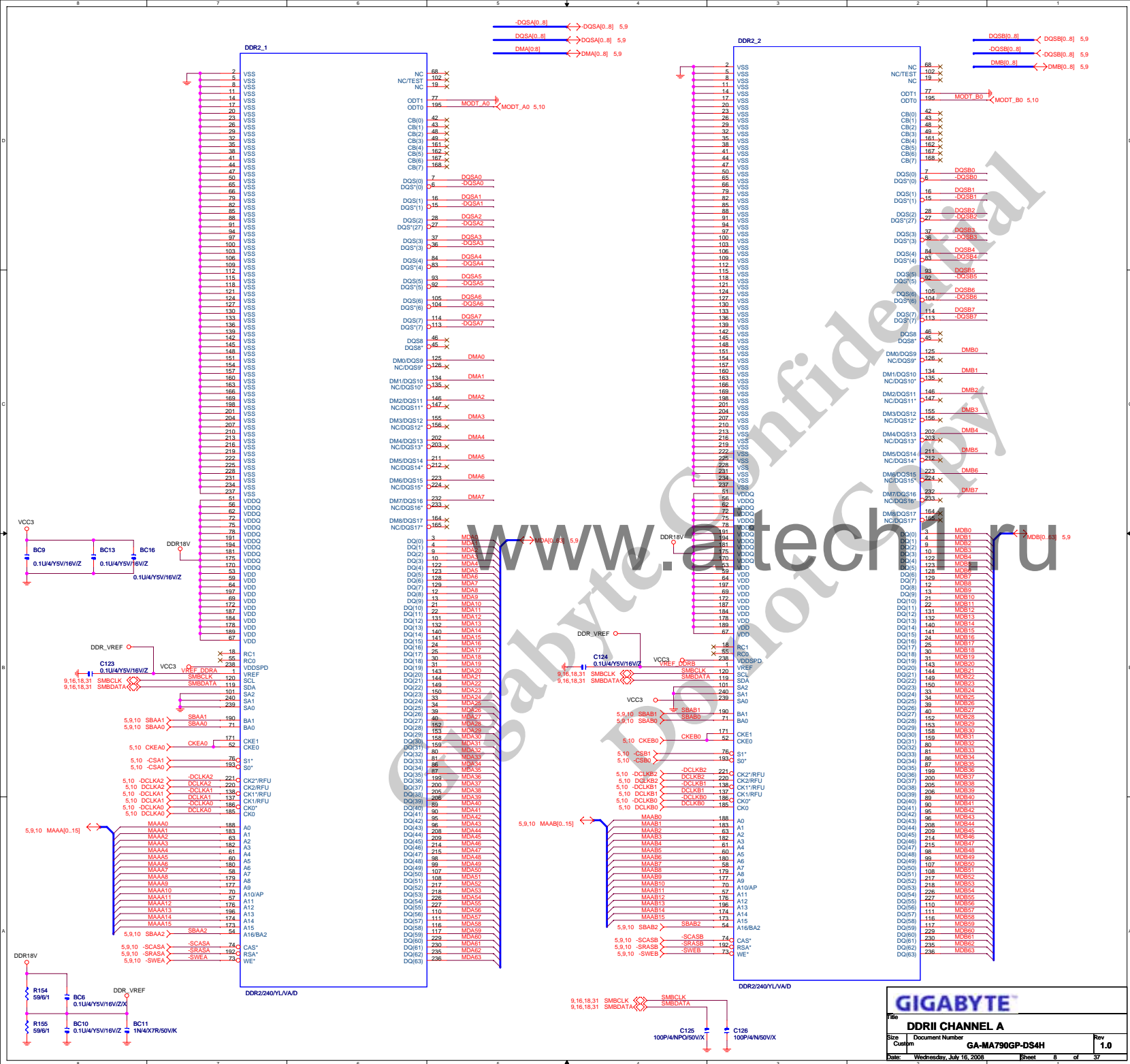
GIGABYTE

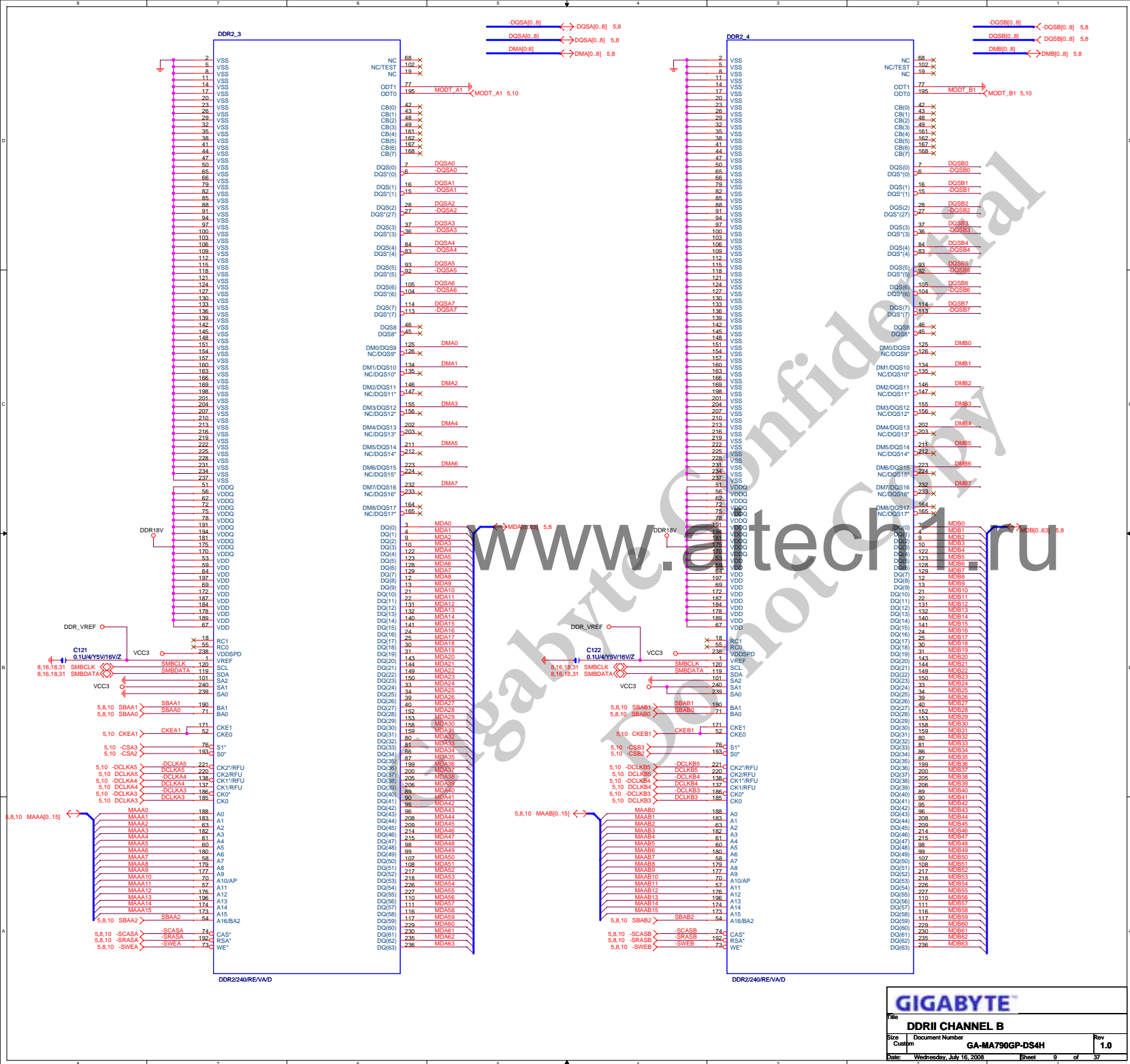
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CPU HYPER TRANSPORT

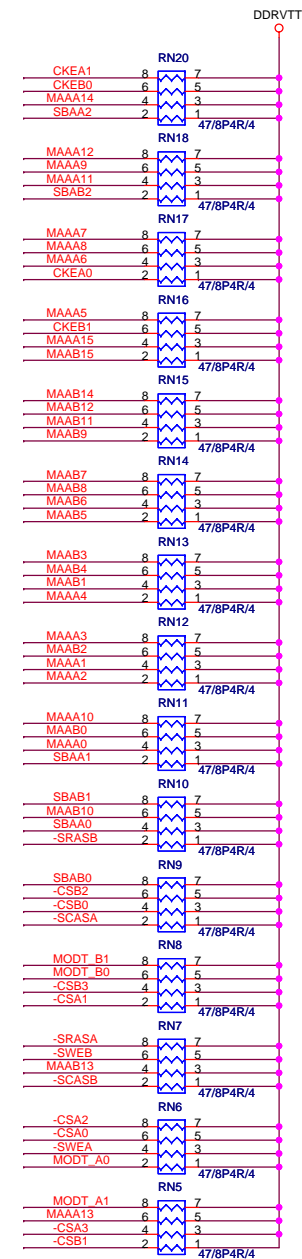
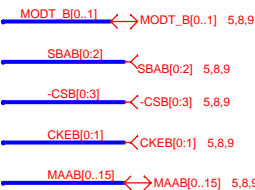
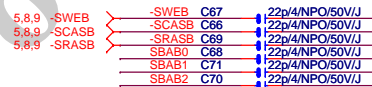
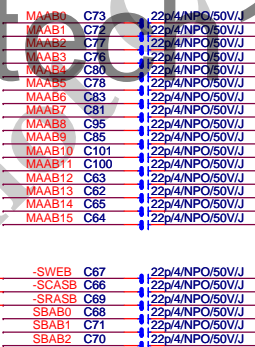
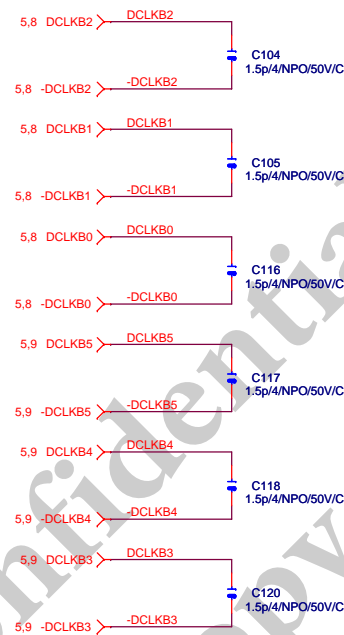
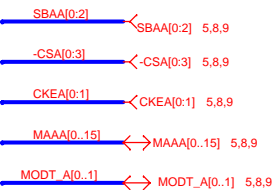
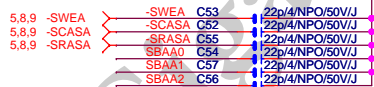
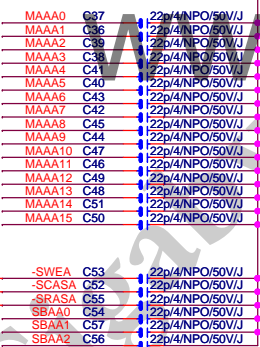
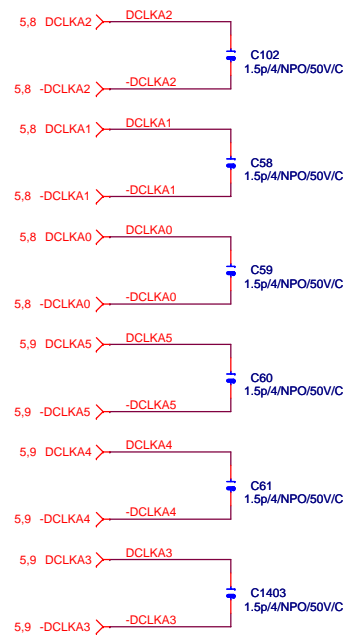
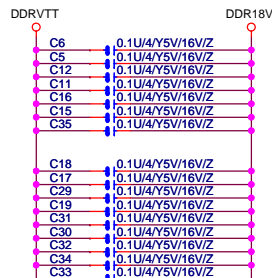
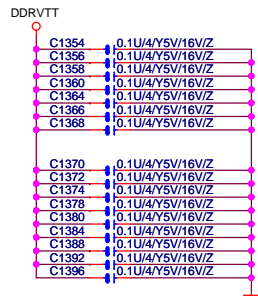
Size Custom Document Number **GA-MA790GP-DS4H** Rev **1.0**

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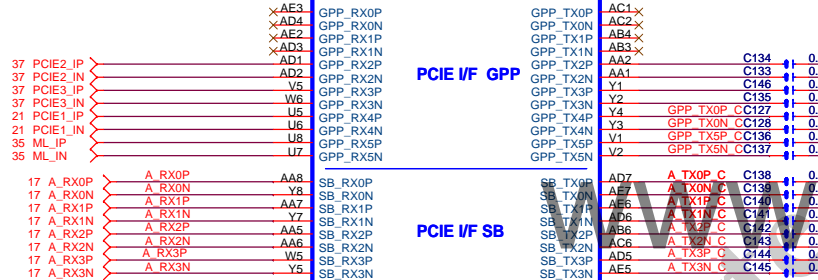
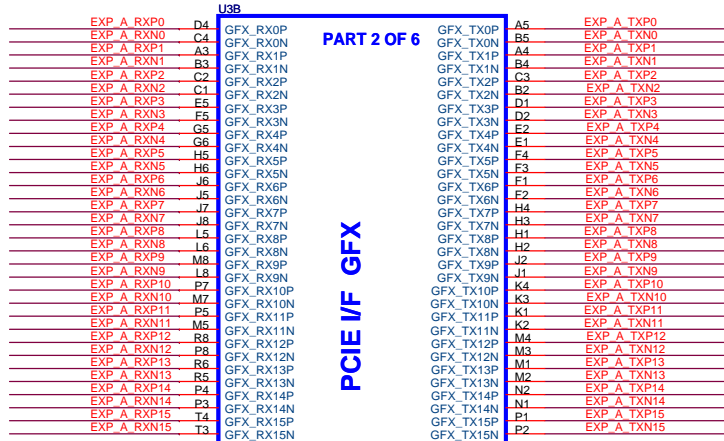






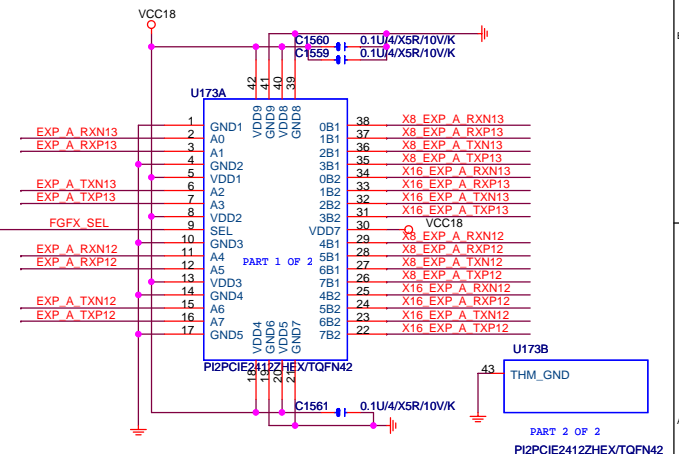
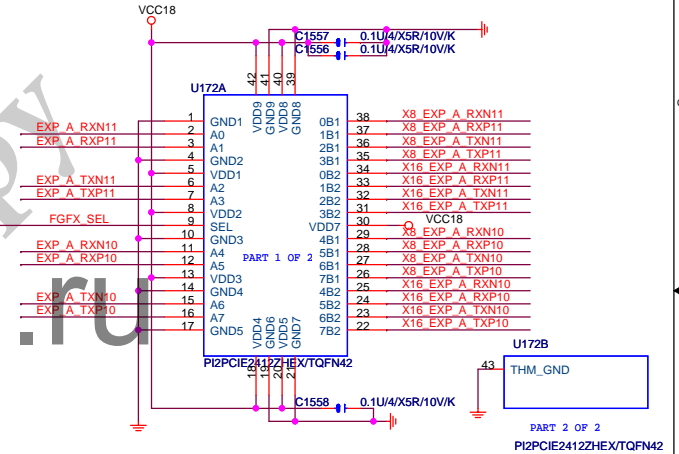
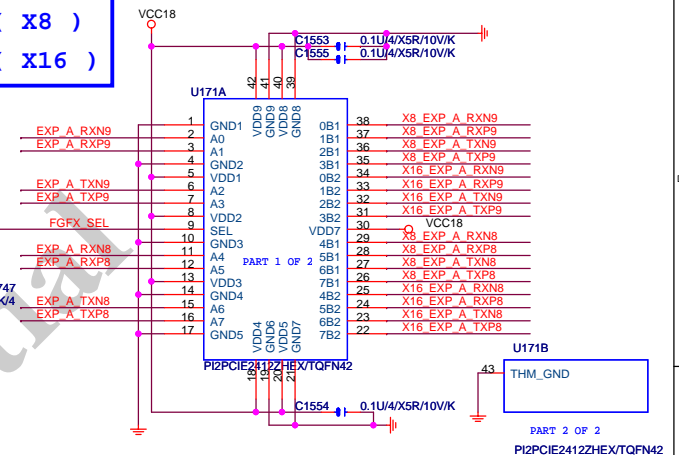
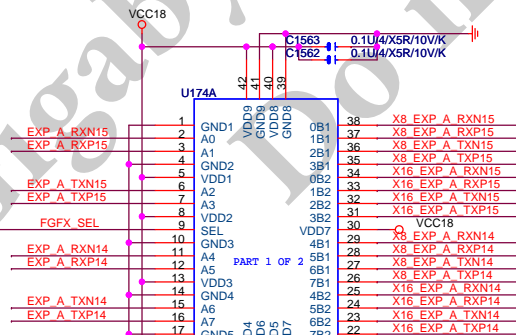
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EXP_A_RXN[0..7] >> EXP_A_RXN[0..7] 21
EXP_A_TXP[0..7] >> EXP_A_TXP[0..7] 21
EXP_A_TXN[0..7] >> EXP_A_TXN[0..7] 21

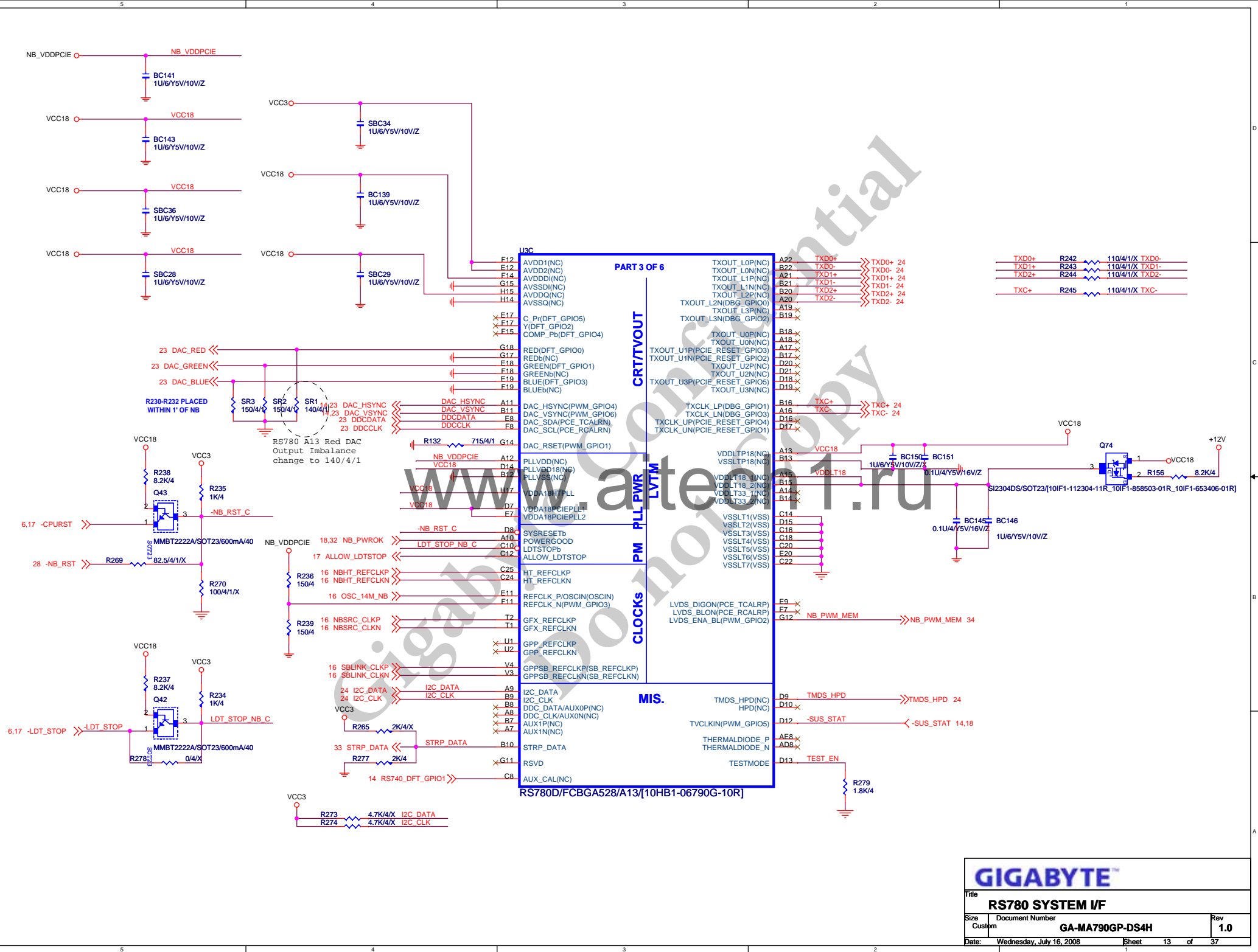
L : A-B1 (X8)
H : A-B2 (X16)

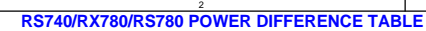


RS780D/FCBGA528/A13[10HB1-06790G-10R]

X16_EXP_A_TXP[8..15] >> X16_EXP_A_TXP[8..15] 21
X16_EXP_A_TXN[8..15] >> X16_EXP_A_TXN[8..15] 21
X16_EXP_A_RXP[8..15] >> X16_EXP_A_RXP[8..15] 21
X16_EXP_A_RXN[8..15] >> X16_EXP_A_RXN[8..15] 21
X8_EXP_A_TXP[8..15] >> X8_EXP_A_TXP[8..15] 37
X8_EXP_A_TXN[8..15] >> X8_EXP_A_TXN[8..15] 37
X8_EXP_A_RXP[8..15] >> X8_EXP_A_RXP[8..15] 37
X8_EXP_A_RXN[8..15] >> X8_EXP_A_RXN[8..15] 37



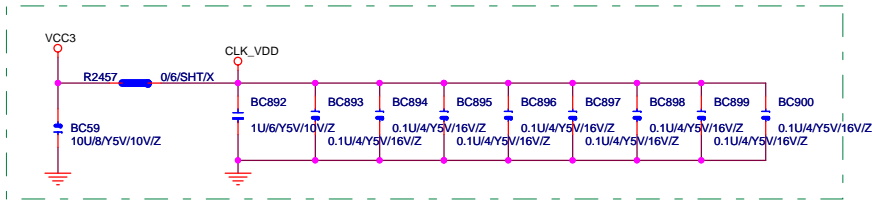




Please use 1mm pad size,
place all ELT test pads
on bottom side only



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- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

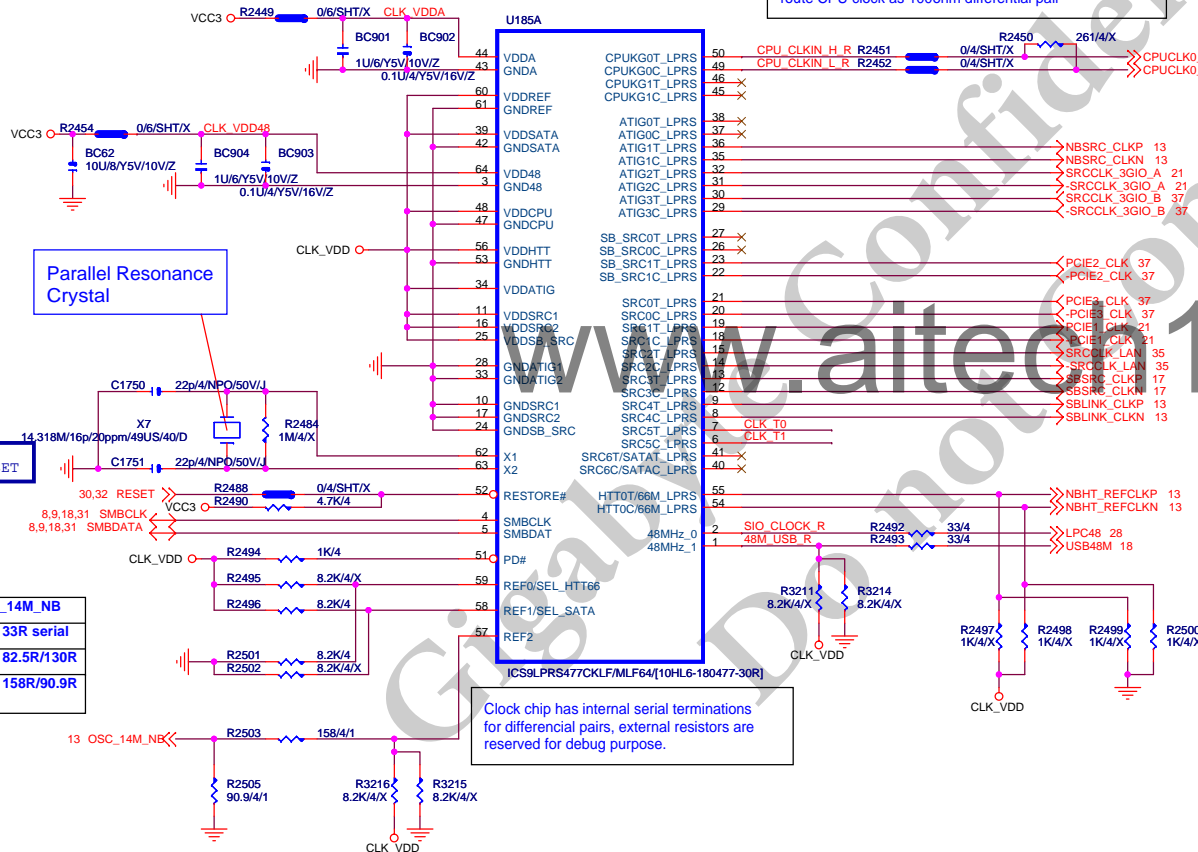


Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



Parallel Resonance Crystal

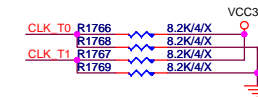
watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

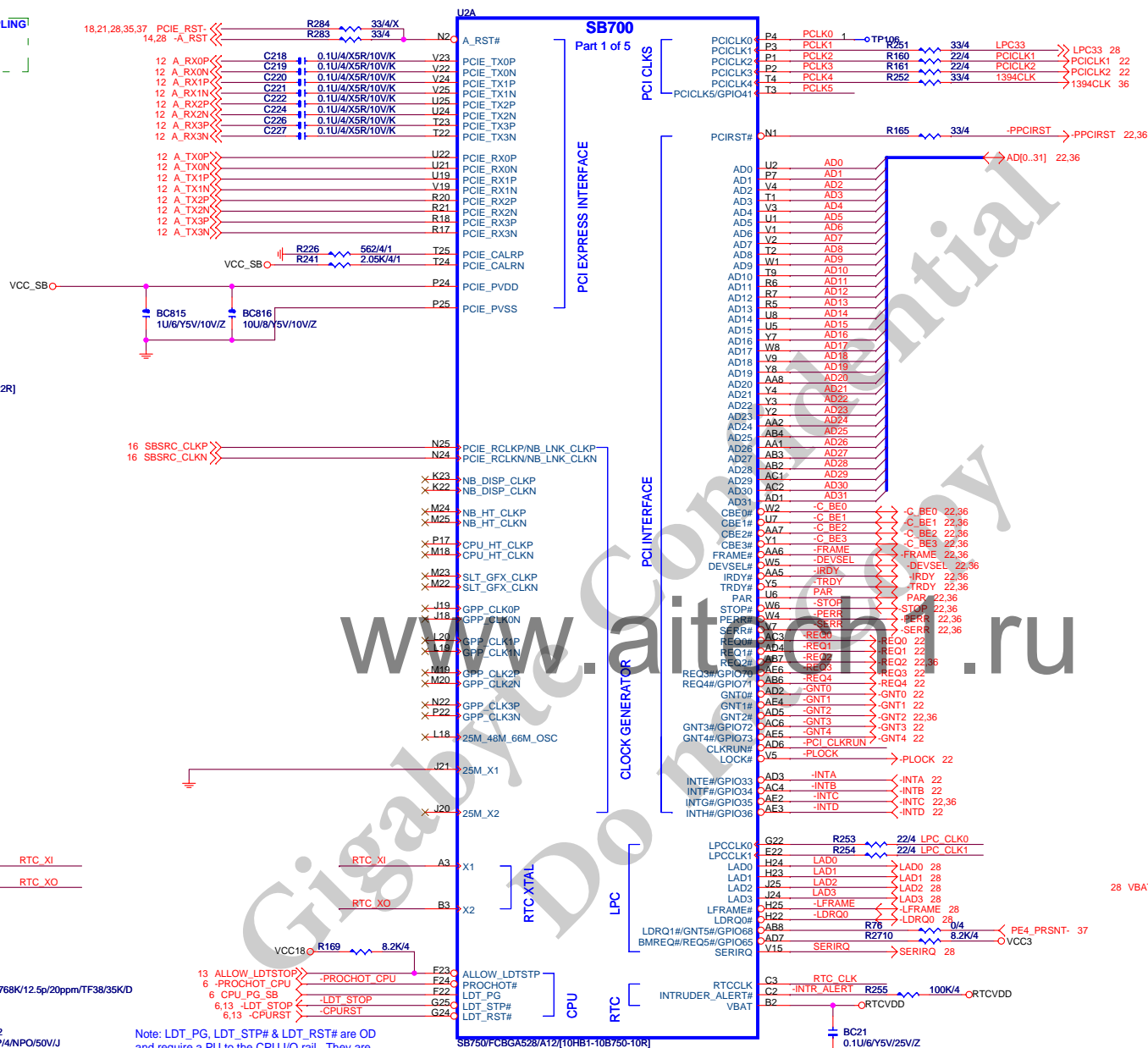
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

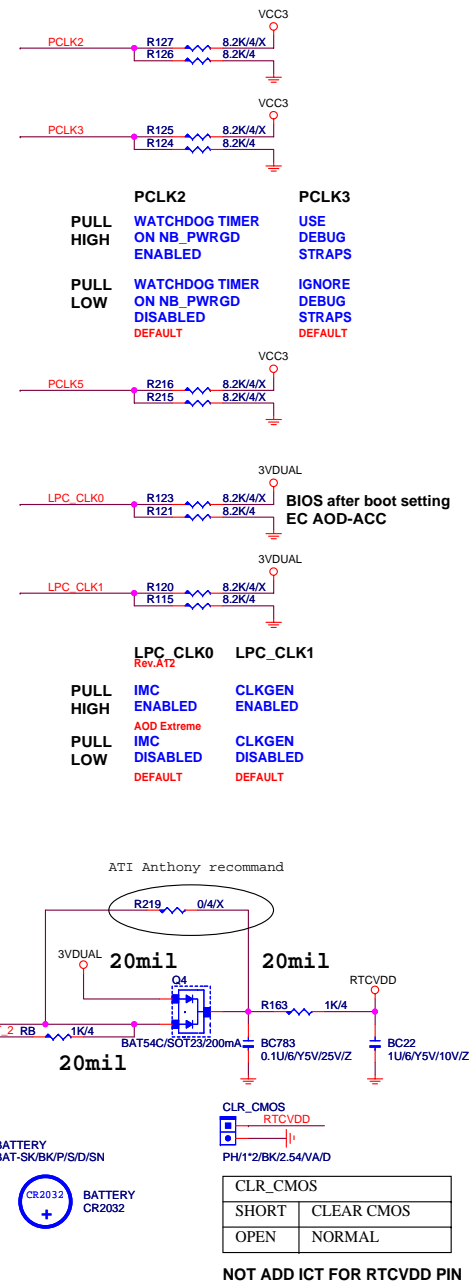
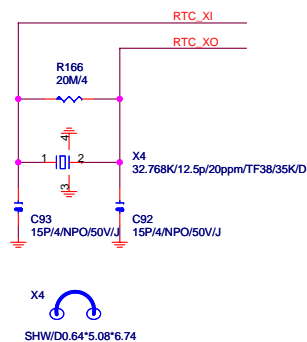




SB_HS/[12SP2-030030-21R_12SP2-030030-22R]



Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.



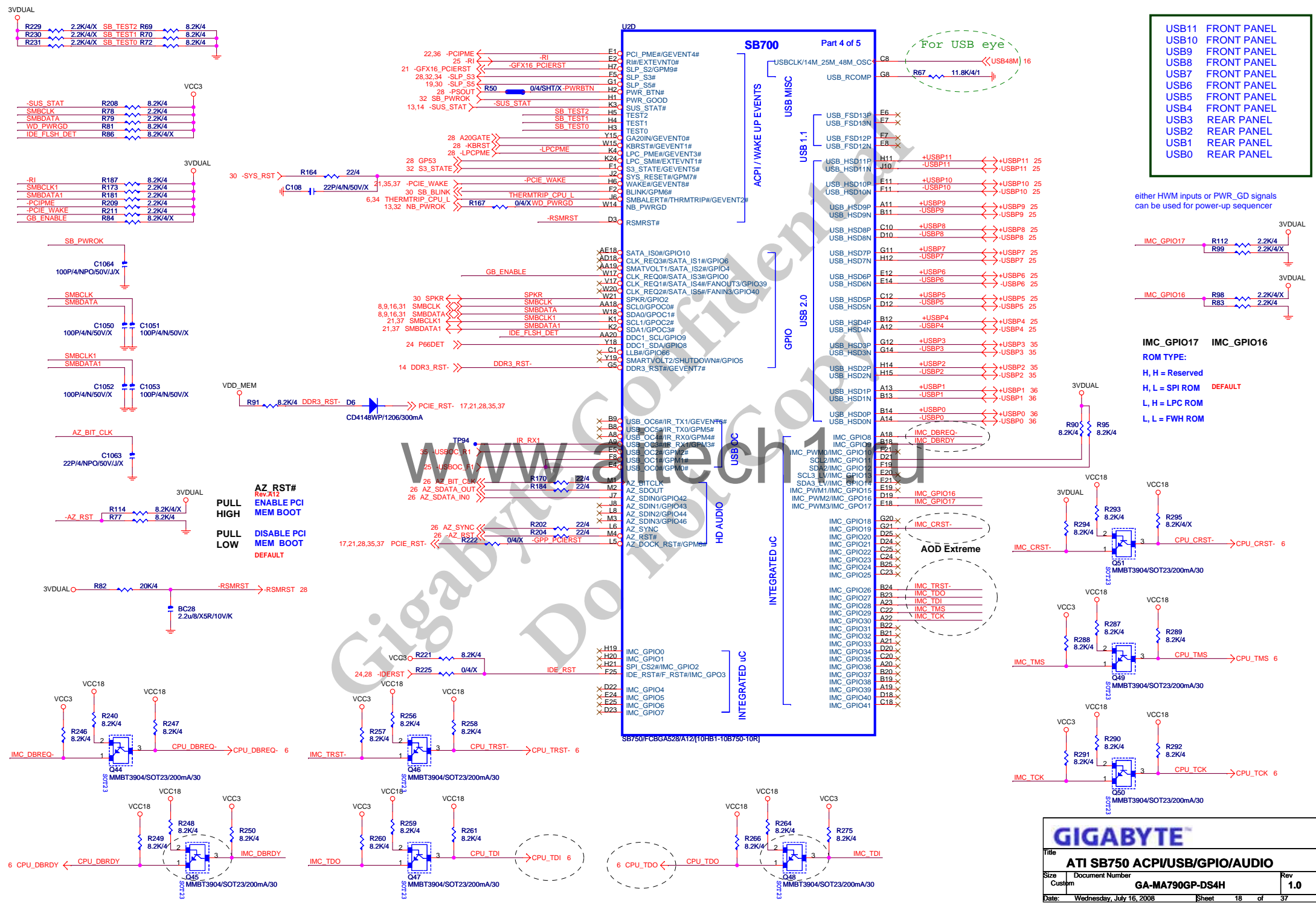
NOT ADD ICT FOR RTCVDD PIN

GIGABYTE™

Title	ATI SB750 PCIE/PCI/CPU/LPC
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Size	Document Number
Custom	GA-MA790GP-DS4H

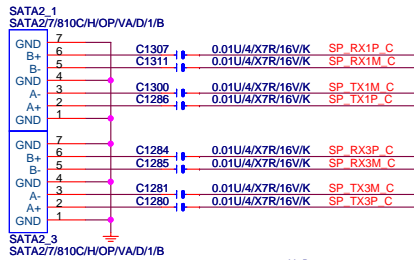
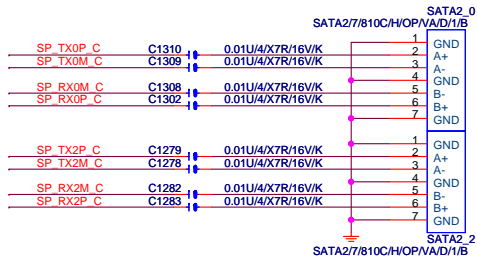
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USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

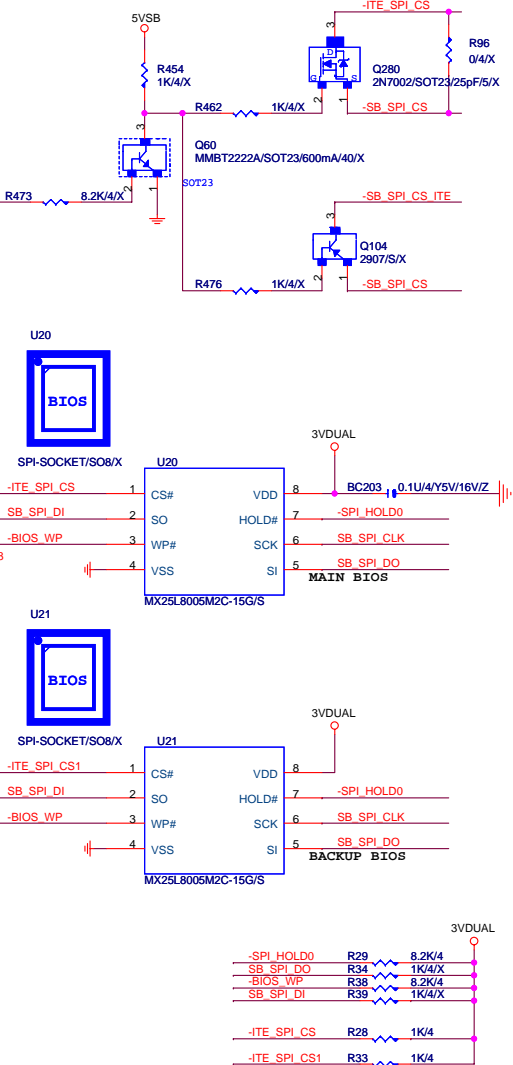
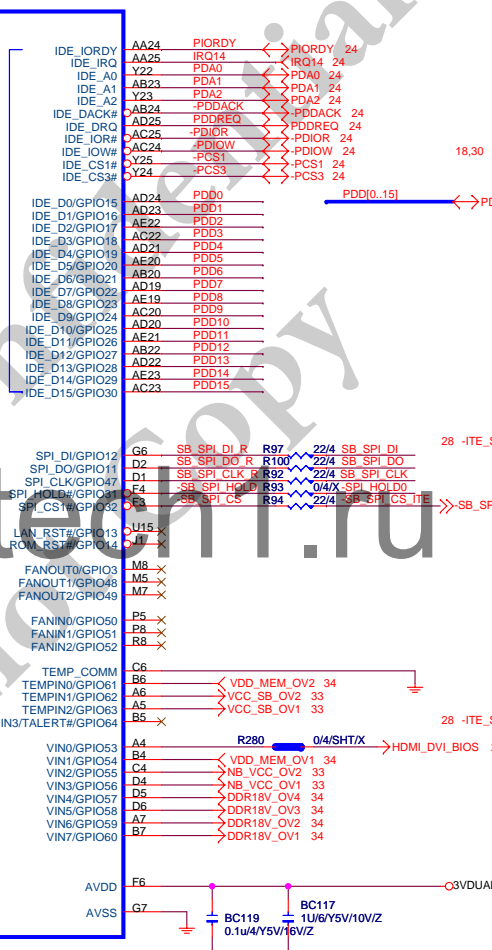
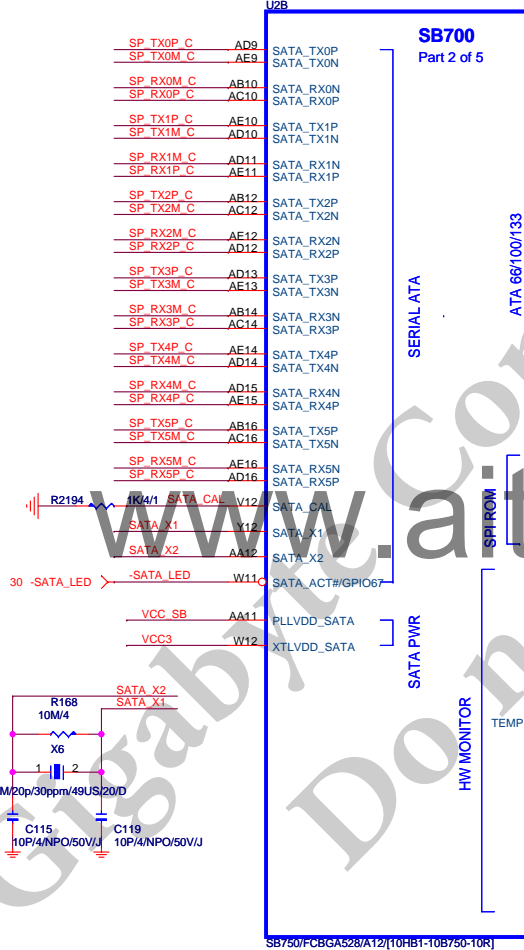
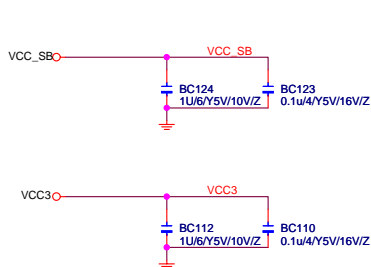
either HWM inputs or PWR_GD signals can be used for power-up sequencer

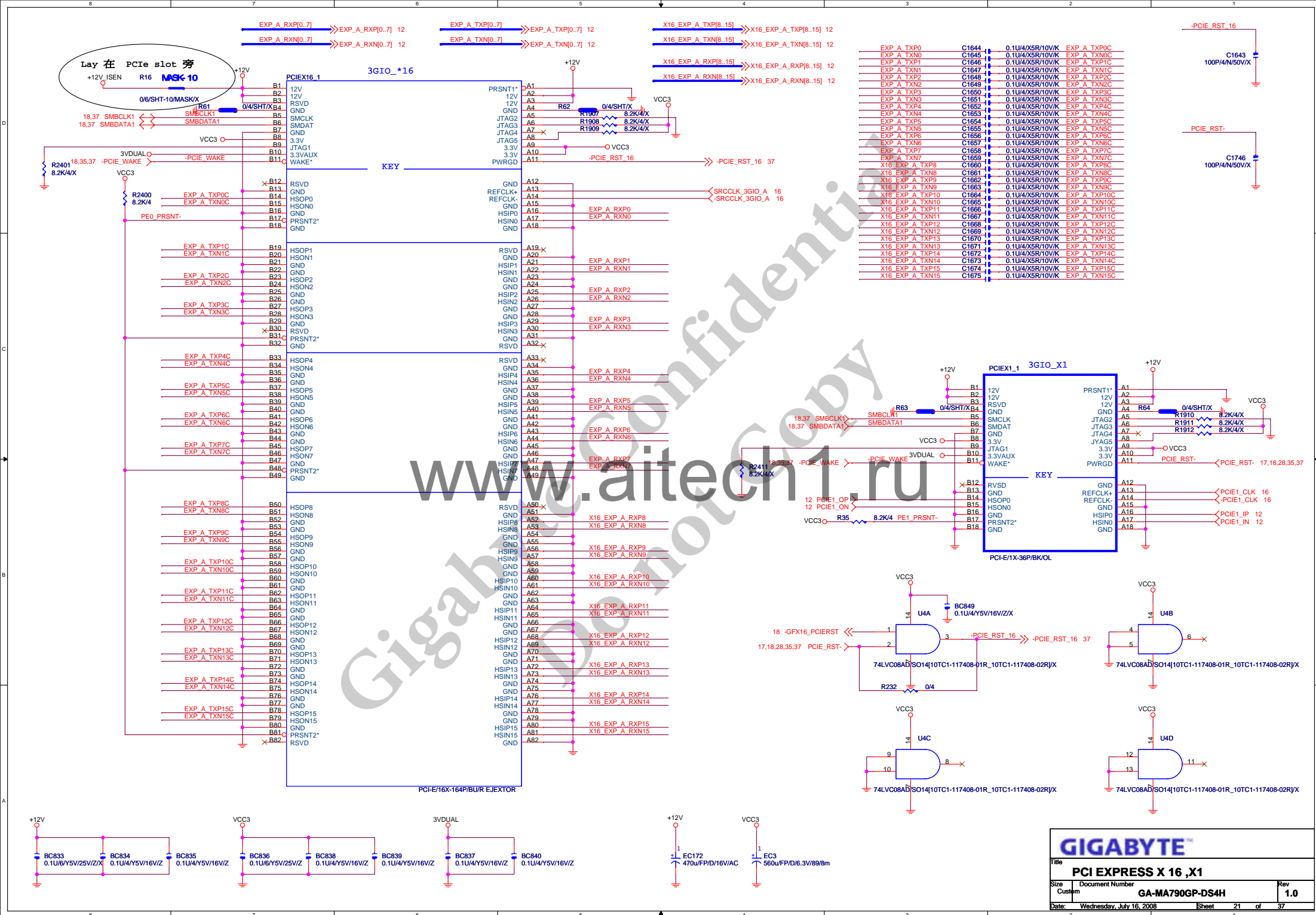
IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM
L, H = LPC ROM
L, L = FWH ROM

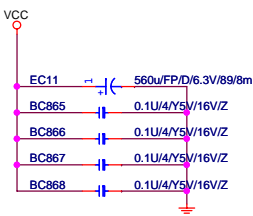
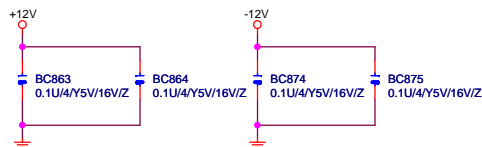
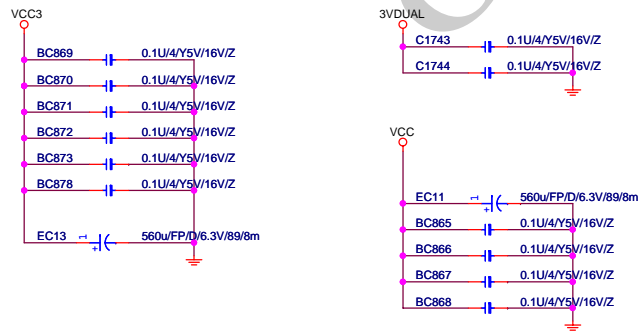
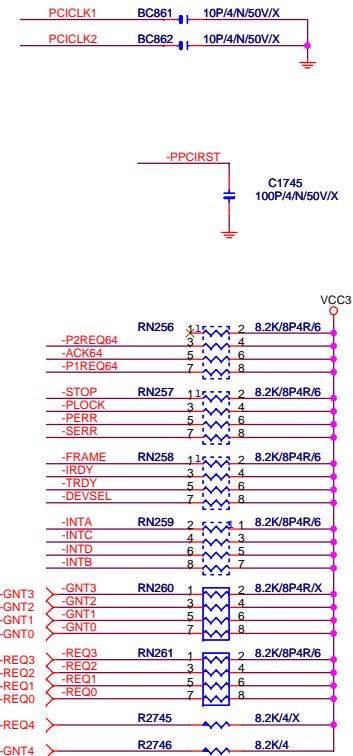
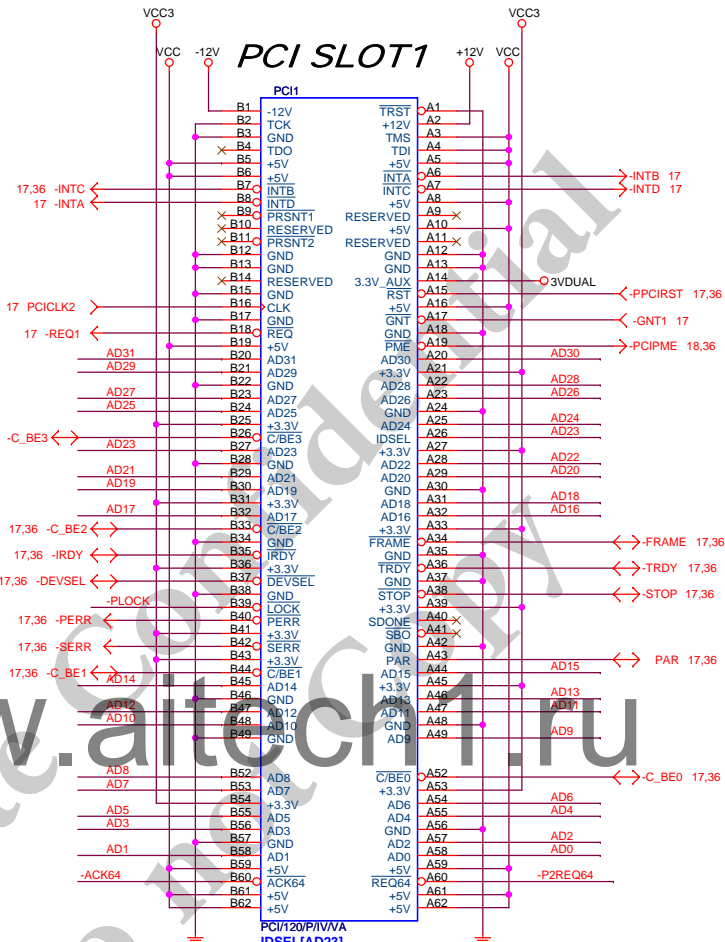
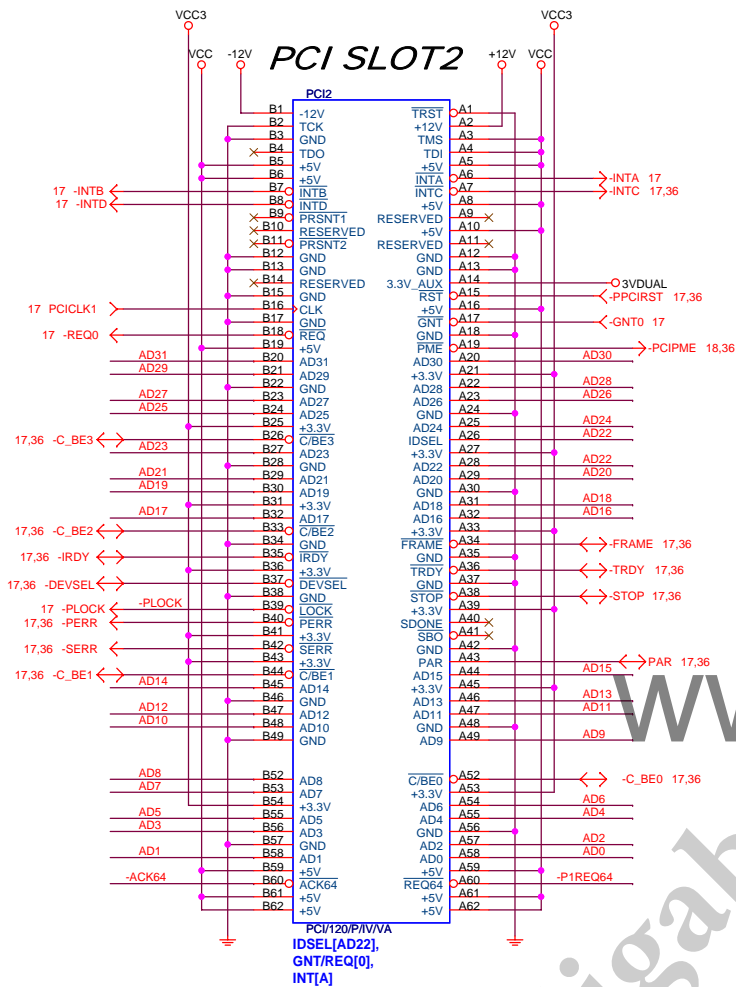


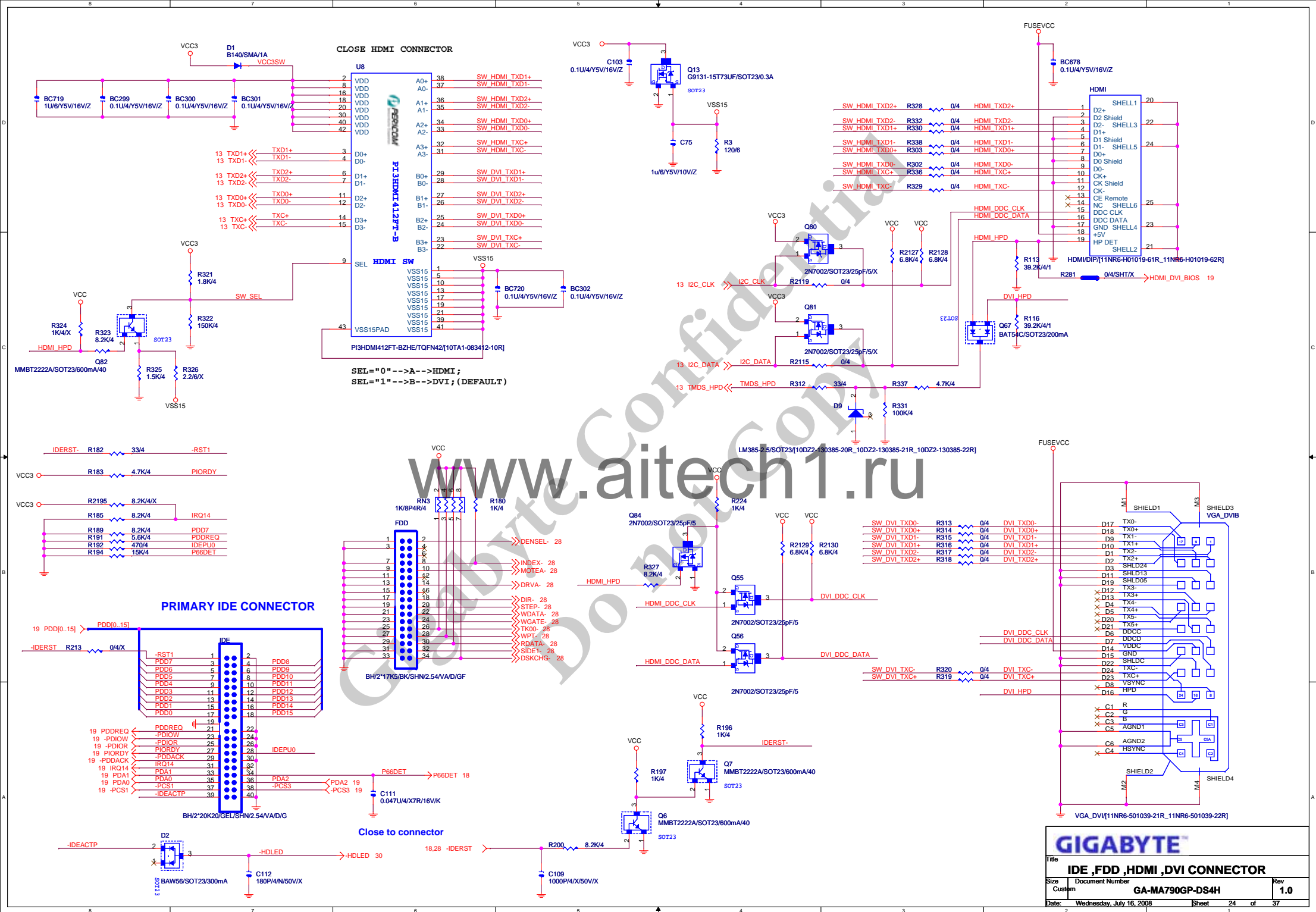
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

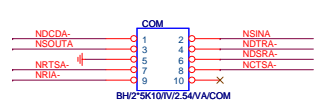
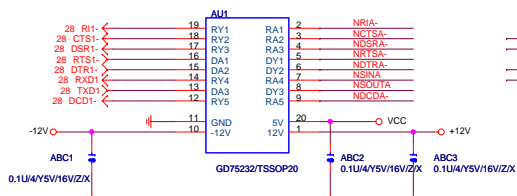
NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK



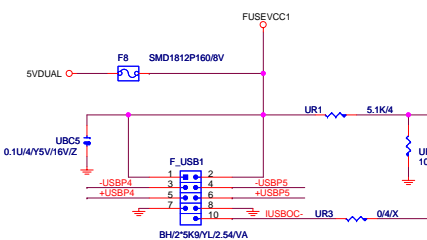




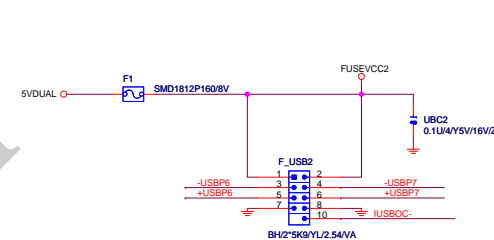




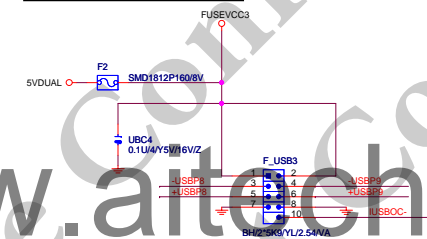
FRONT SIDE USB1



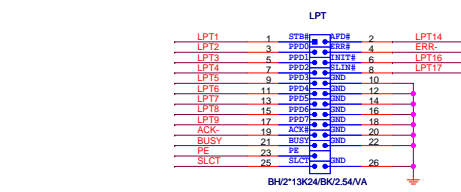
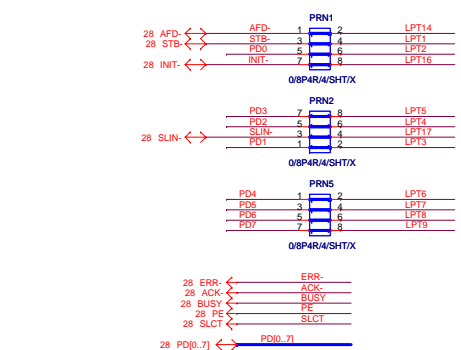
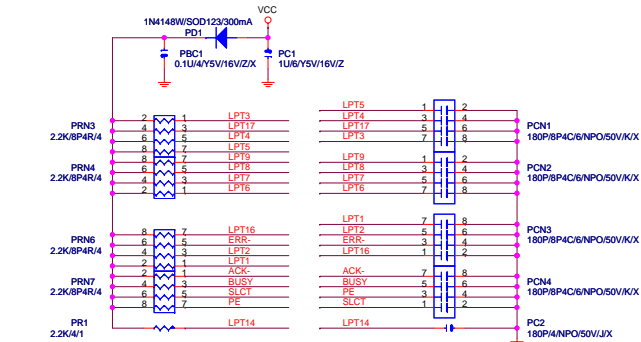
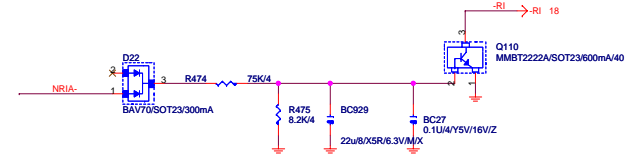
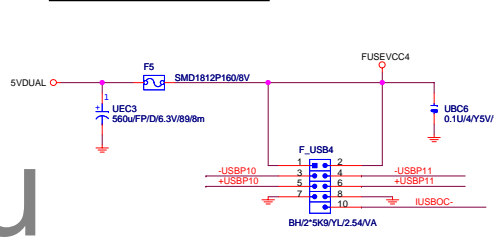
FRONT SIDE USB2

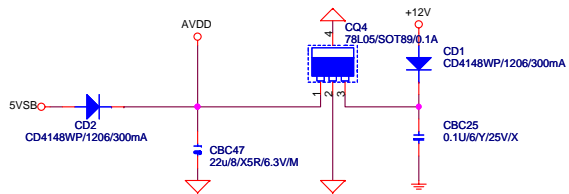
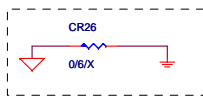


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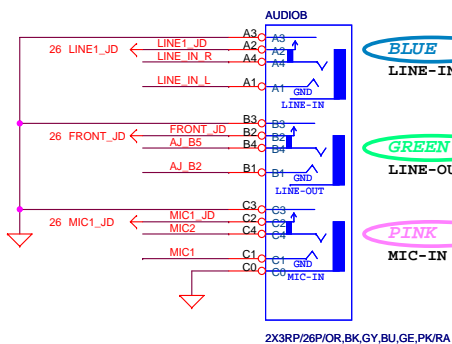
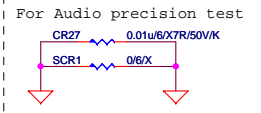
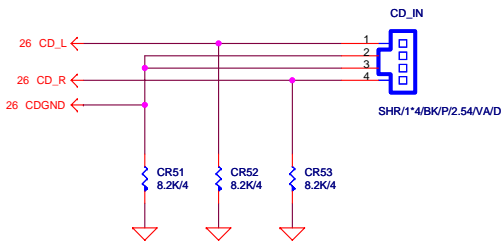


FRONT SIDE USB4



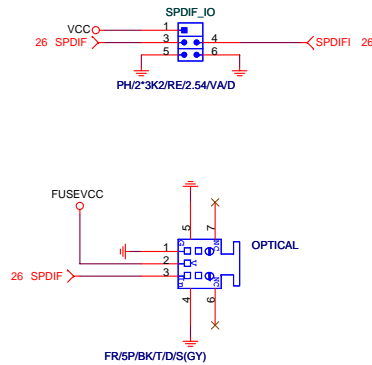


CD IN

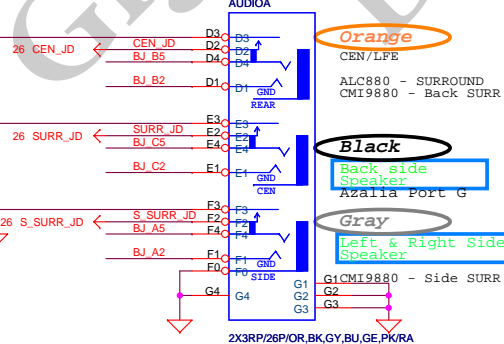
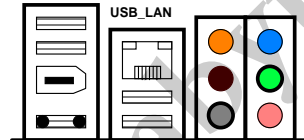


A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ*15P/[11NR6-403004-11]

SPDIF

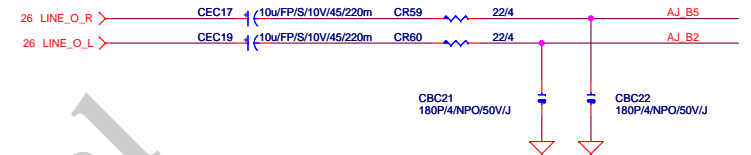


USB_1394_ESATA

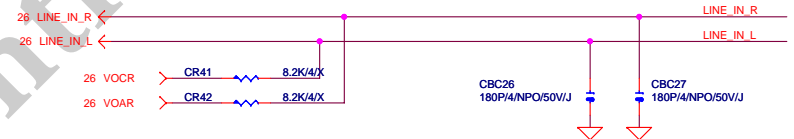


A3RJ/13P/0BG/[11NR6-403006-71]
3RJ*15P/[11NR6-403004-31]

LINE OUT FRONT OUT



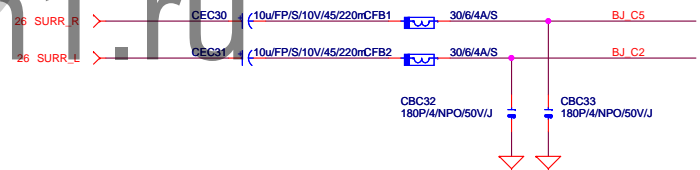
LINE-IN



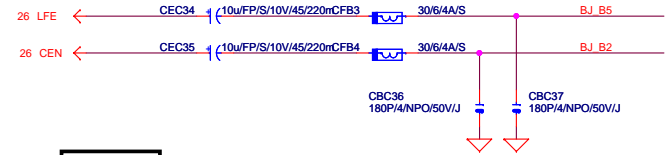
MIC



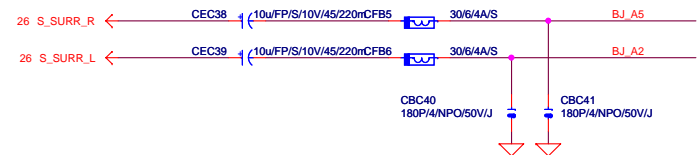
SURROUND



CEN/LFE

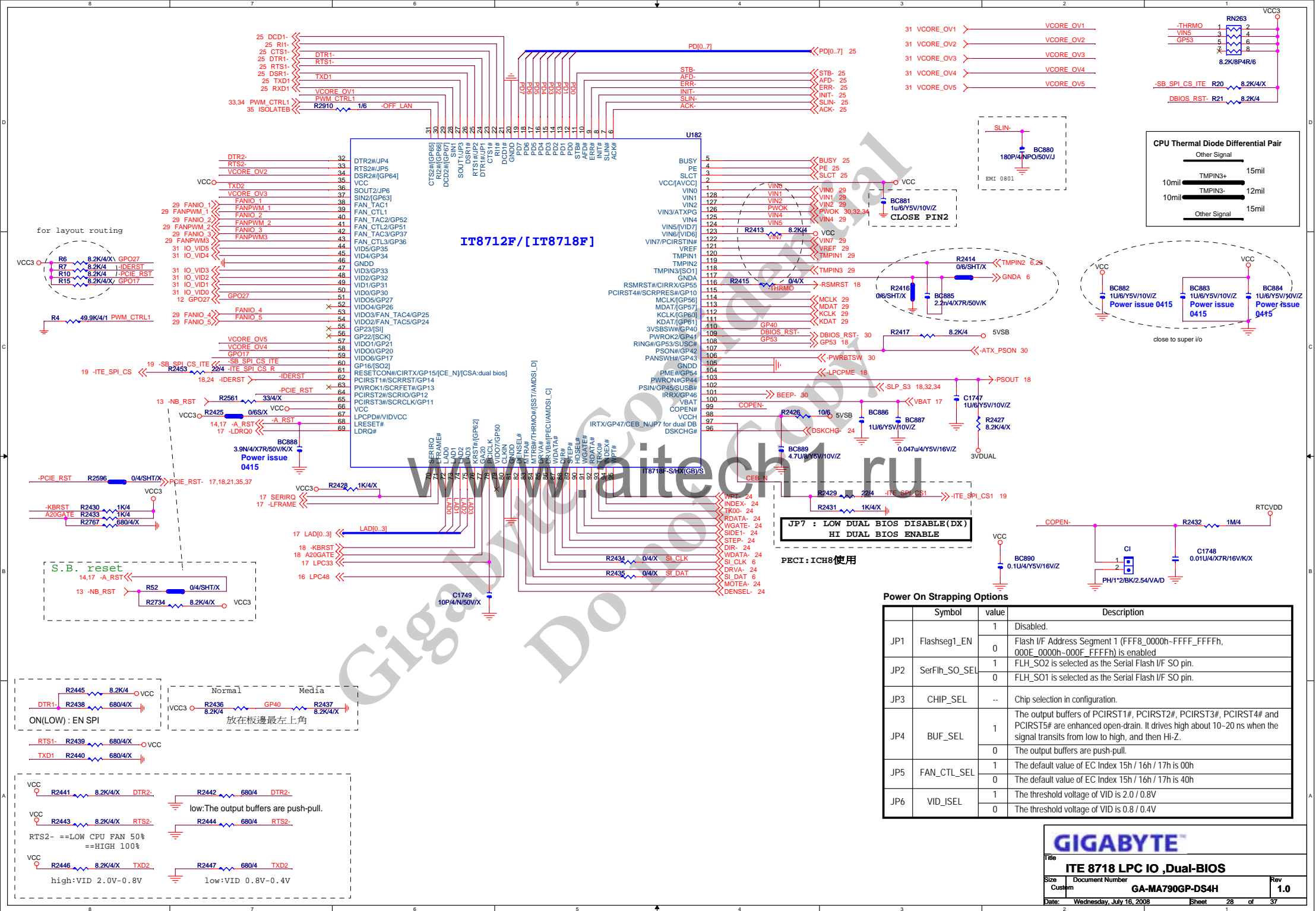


SURR BACK

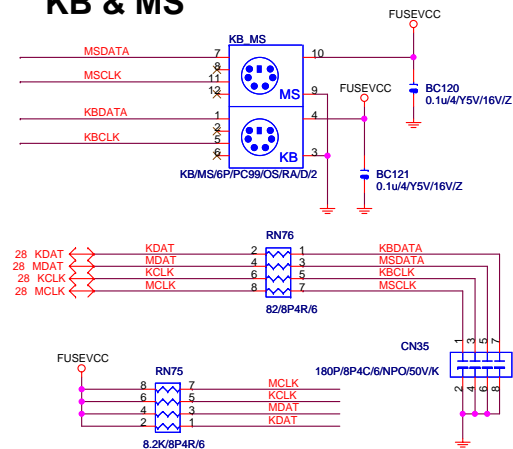
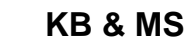
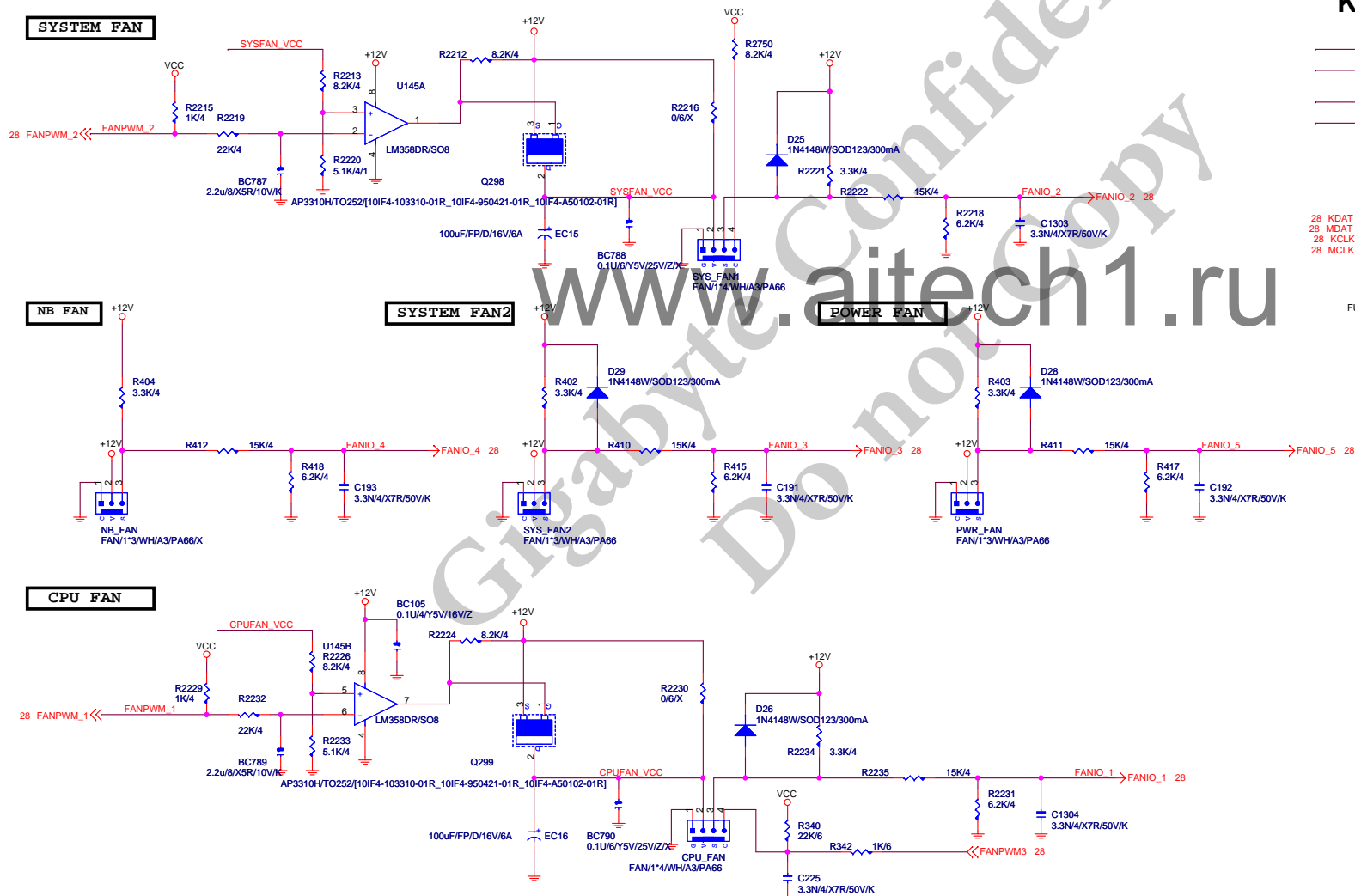
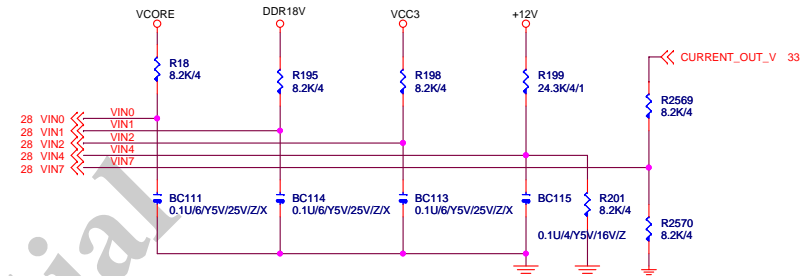
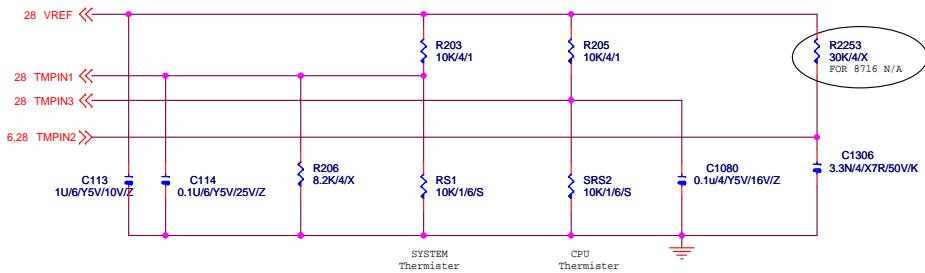


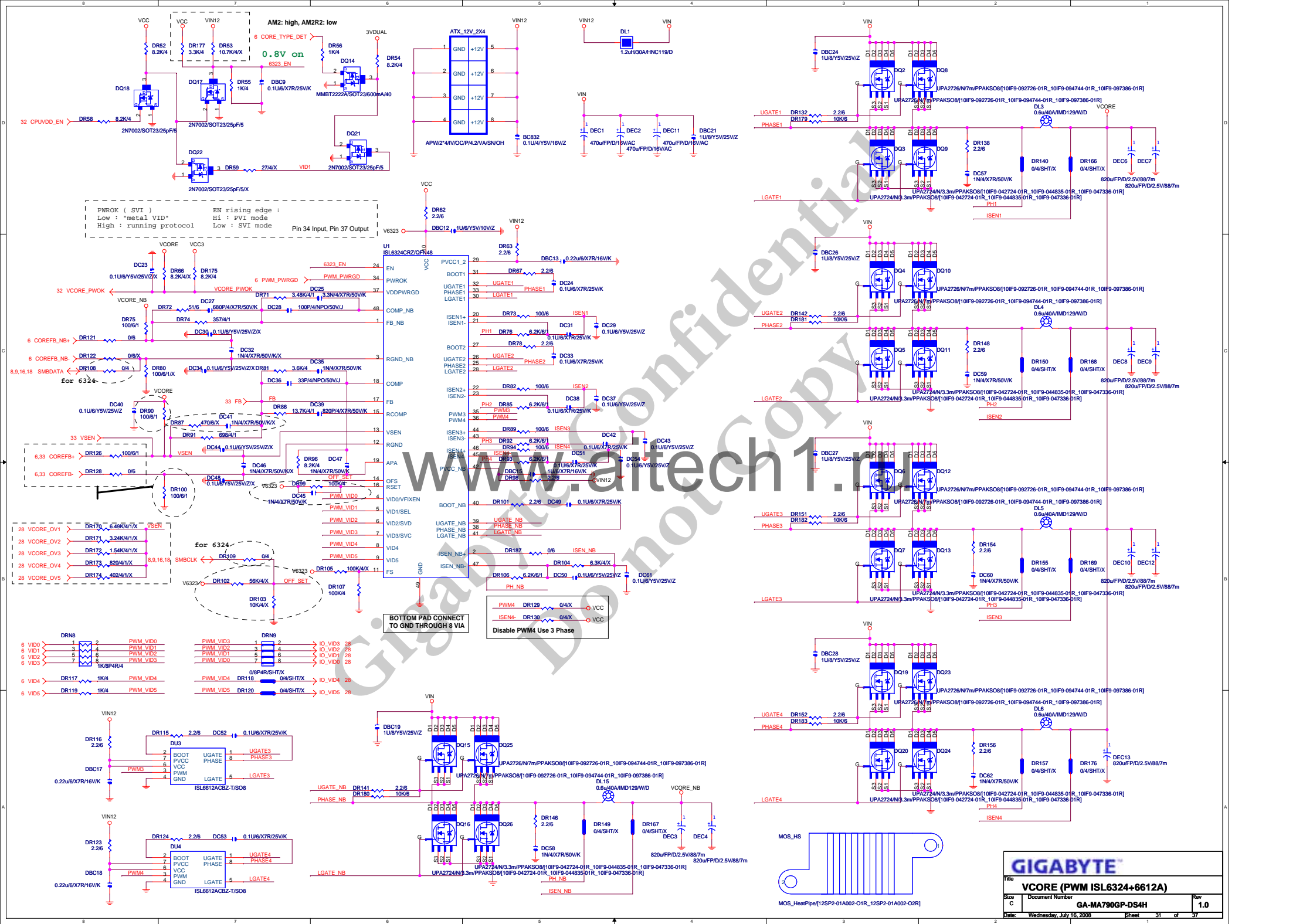
GIGABYTE

Title		
AUDIO JACK		
Size	Document Number	Rev
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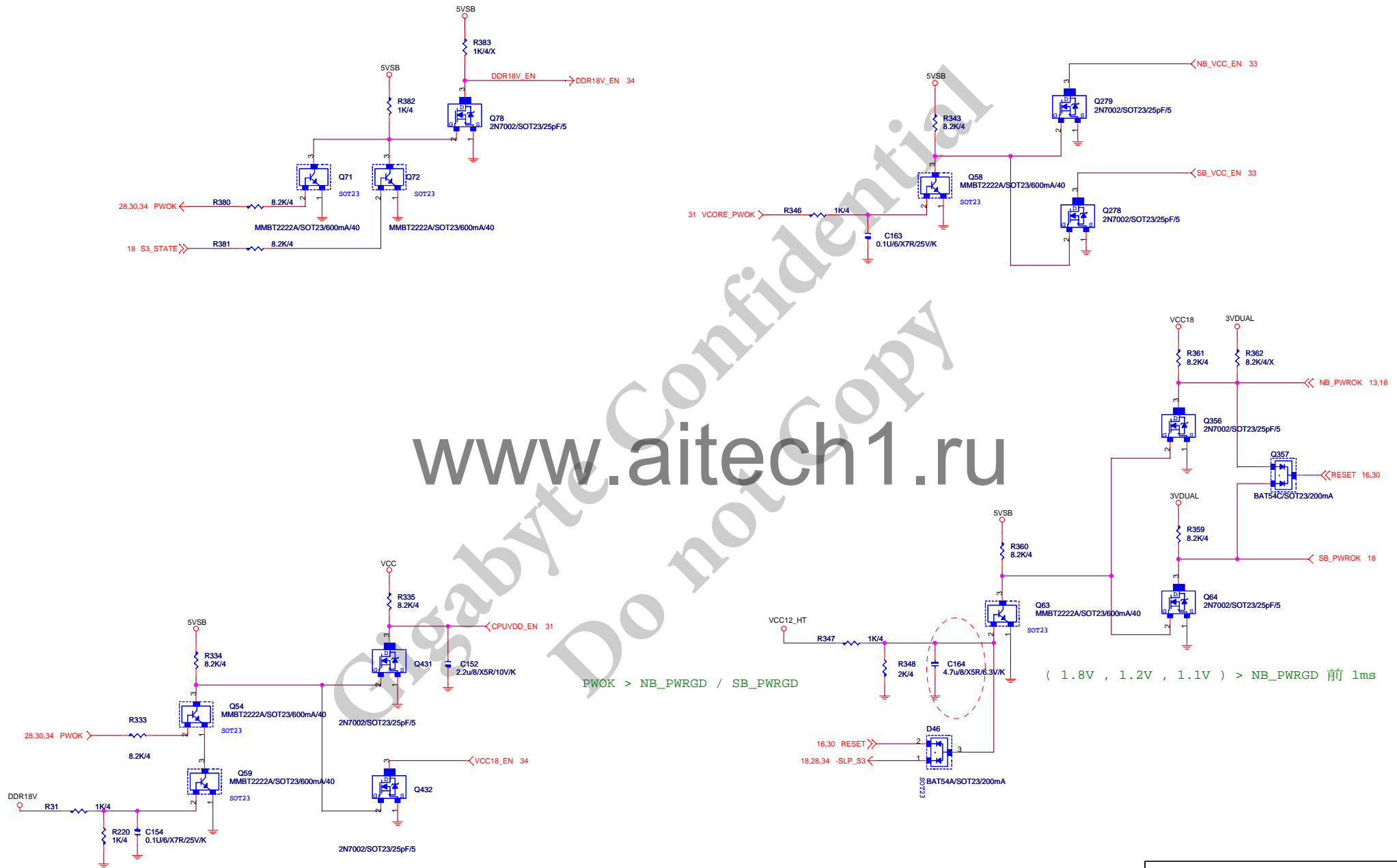


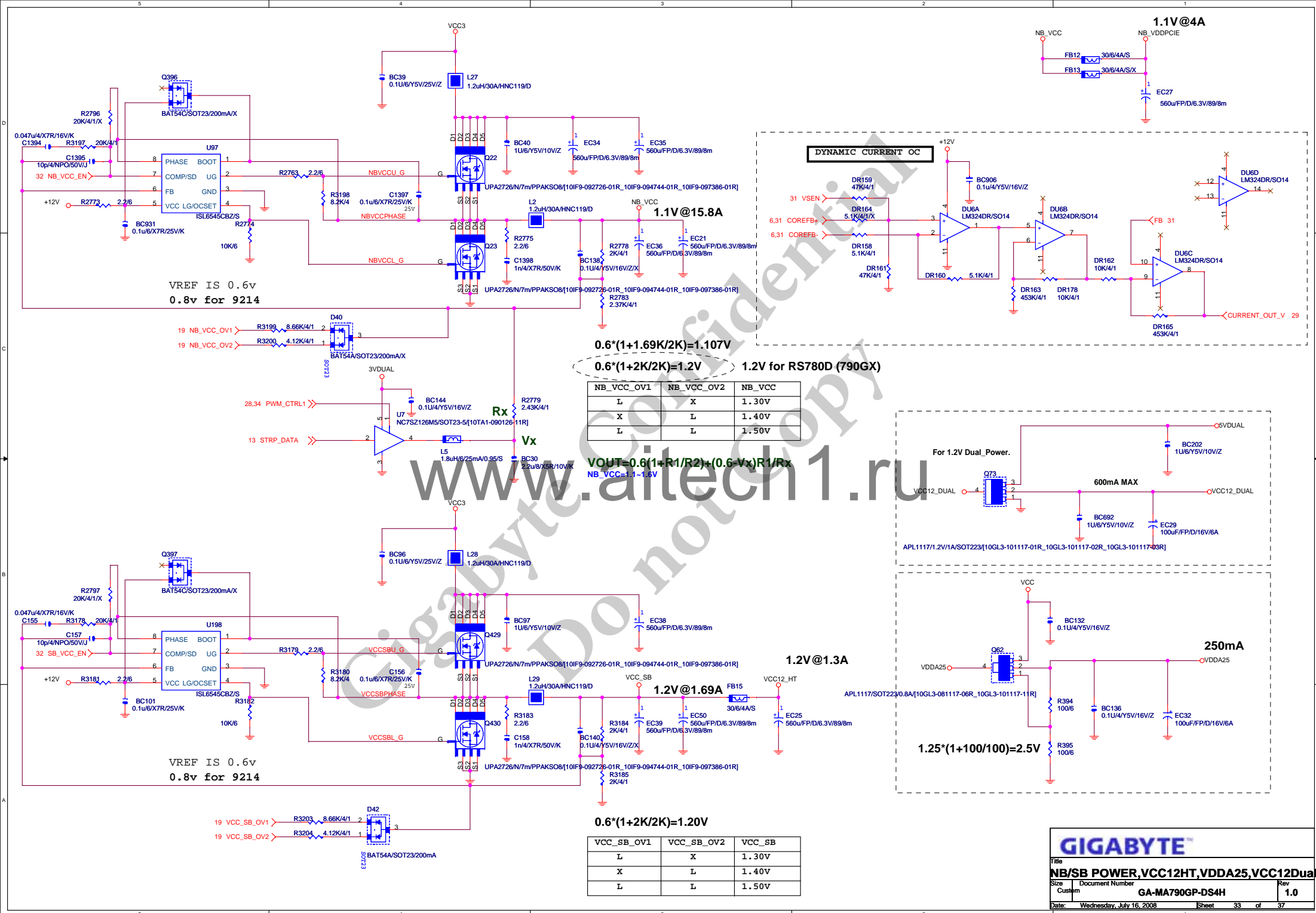
Hardware Monitor circuits



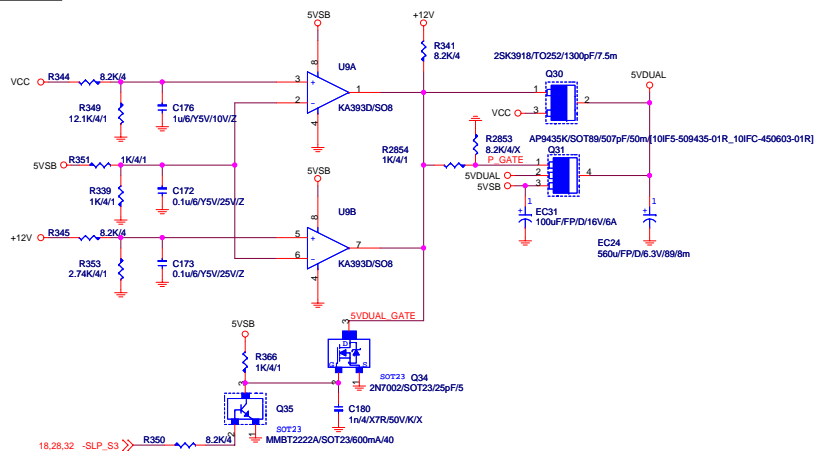


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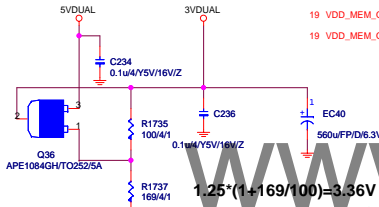
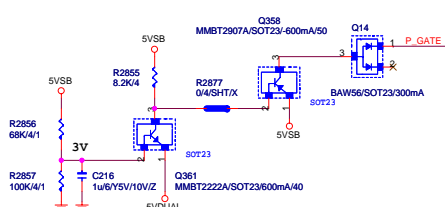




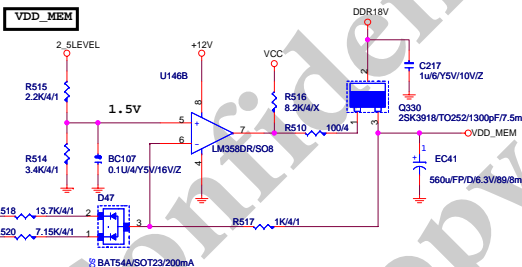
5VDUAL



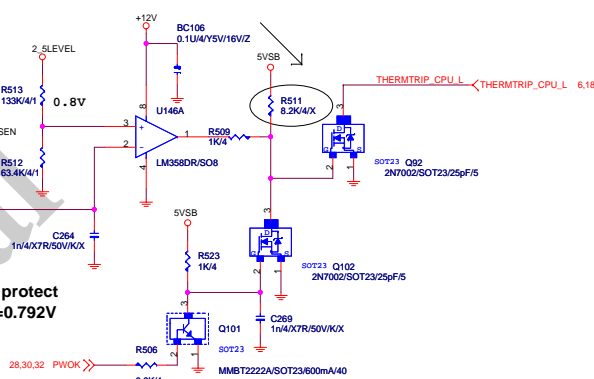
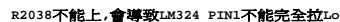
3VDUAL



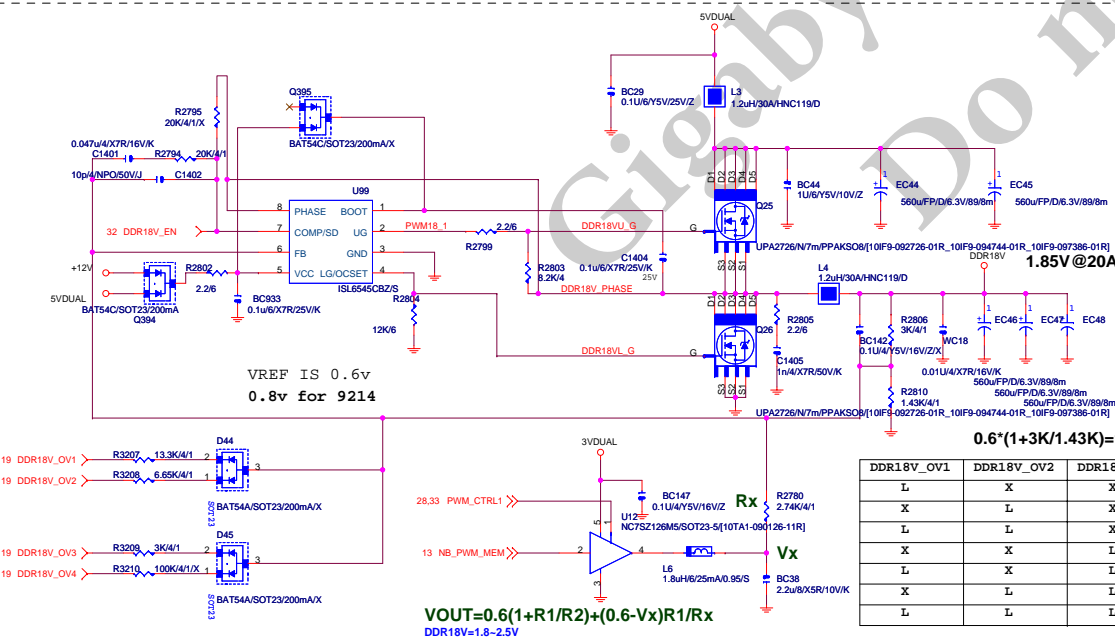
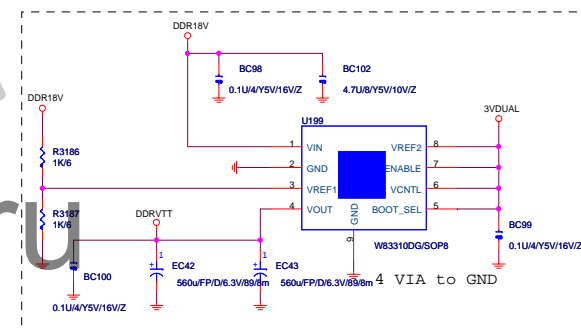
VDD_MEM



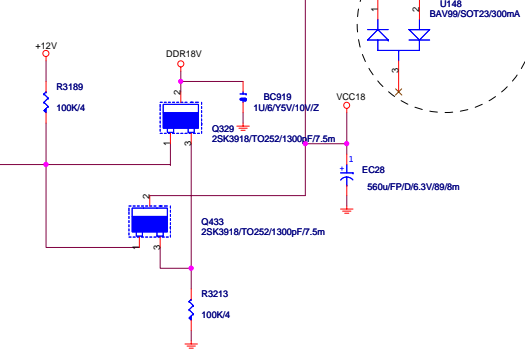
VDD_MEM_OV1	VDD_MEM_OV2	VDD_MEM
L	X	1.60V
X	L	1.70V
L	L	1.80V



9.5V / 25A protect
 $9.5 \times (1.21K / (13.3K + 1.21K)) = 0.792V$



ATI for vcc3/vcc18 power ramp-up 2.1V



DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V
L	X	X	1.90V
X	L	X	2.00V
L	L	X	2.10V
X	X	L	2.20V
L	X	L	2.30V
X	L	L	2.40V
L	L	L	2.50V

